REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claims 1-12 were presented for consideration in this application. By the foregoing amendment, Applicant has amended Claims 1 and 12. New Claims 13-20 have been added. Claims 1-20 are now pending.

In the specification, paragraphs on page 1 and 11 have been amended to update cross-referenced serial numbers. Paragraphs [28], [80] and Table 2 have been amended to correct minor editorial problems. A replacement Abstract is provided that has a word count less than 150 words.

In the Figures, Figures 6, 10, and 13B are amended to correct/add reference numbers.

In the Claims, Claim 12 is amended to correct terminology, as noted by the Examiner.

Rejections

Claims 1-3, 5-9, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hassoun et al. (5,557,622).

Claims 4 and 10-11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Hassoun et al.

The rejections are based on Hassoun which teaches only cached systems. Hassoun's cache performs block reads to update the cache if a miss occurs or block writes to remove dirty data from the cache, as is commonly done in cache systems. (col. 5, lines 5-14) Conversely, Applicant's novel "local memory" is not a cache system, in that it does not overlay a portion of secondary memory, but is instead an independent portion of memory that occupies its own portion of the address space of the processor, as discussed in the specification at paragraph 81 and elsewhere. Claim 1 recites "local memory" and has been amended to make clear that the

local memory "occupying a portion of the address space of the processor" is not the same as a cache. Claim 1 is allowable over Hassoun for this reason.

Furthermore, Claim 1 recites: "...the DMA circuitry operable to transfer data to a **selectable** portion of segments of the plurality of segments from a **selectable** region of a second memory..." in the commonly understood manner that DMA circuits are programmed to select both the location to transfer from and the location to transfer to. Conversely, Hassoun's cache fill "is completed using the known direct memory access (DMA) technique controlled by the signals at the bus request and bus grant terminals (445) of the control logic element (440). (Col. 7, lines 6-9) Hassoun's cache fill is completely determined by the original memory request from the processor and is in no manner "selectable" in the sense that is claimed in Applicant's Claim 1. Thus, Hassoun does use a DMA technique to complete a cache fill as is commonly done in caches, but this is in no way equivalent to a "DMA circuit" that can be programmed to select a source and destination for transfers, as is commonly understood for "DMA circuits" and described with respect to Applicant's Figures 13A and 13B. Claim 1 is therefore allowable over Hassoun for this additional reason.

Dependent Claims 2-11 depend directly or ultimately on allowable base Claim 1 and are therefore allowable for this reason and by virtue of their further distinctive recitations. For example, Claims 2 and 7 both relate to aspects of a programmable DMA circuit in the sense discussed above that sets either valid bit and/or dirty bits. Hassoun does not suggest any sort of programmable DMA circuit.

Claim 4 recites: "...whereby the timeout circuit is operable to interrupt the processor if the DMA circuitry does not validate the first segment within a certain period of time." The Examiner admits Hassoun does not suggest such capability, but suggests such operation is obvious. Applicant respectfully disagrees that such operation is obvious in that Hassoun's memory is a cache and caches operate in an autonomous manner, ie, they perform a cache fill automatically in response to a cache miss. Therefore, there is no reason that a cache as taught by Hassoun would not be filled in a timely manner, other than in a true error situation. Conversely, Applicant's DMA circuit with selectable source and destination is programmed separately and may or may not be ready to transfer data when the processor reads "the first segment." Claim 4 is allowable over Hassoun for this additional reason.

Claim 6 recites: "the DMA circuitry is operable to transfer a block of data to the selected portion of segments in such a manner that a transfer to the first segment holding valid data within the selected portion of segments is inhibited." In other words, within a selected block of data, segments that are indicated as being valid are not transferred by the DMA circuitry, but other segments that are marked as being invalid are transferred all within a single block transfer. Conversely, Hassoun either transfers the whole block, or nothing. (Col 2, lines 45-61) Claim 6 and similarly Claims 8 and 10 are allowable over Hassoun for this additional reason.

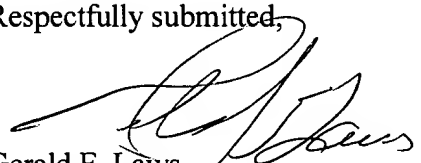
Independent method Claim likewise refers to "a local memory" and has been amended to make clear that it "occupies a portion of the address space of the processor." As discussed above, Hassoun does not teach anything regarding local memories, only cache memories. Claim 12 is allowable over Hassoun for the reasons discussed above.

Applicant has now presented new dependent method Claim 13-20 in order to more fully protect Applicant's contribution to the art. Dependent Claims 13-20 depend directly or ultimately on allowable base Claim 12 and are therefore allowable for this reason and by virtue of their further distinctive recitations for the reasons discussed above.

Applicant believes this application and the claims herein to be in a condition for allowance and respectfully requests that the Examiner allow this application to pass to the issue branch.

Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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